IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) A device to manage a plurality of arithmetic flags, wherein an M-bit set of arithmetic flags is associated with each of a plurality of data items of varying field sizes within words of N bits, ~~an N-bit word,~~ M and N being positive integers, comprising:

a combination function module to examine one of the N-bit words ~~a word~~ comprising a plurality of sets of arithmetic flags, to determine a data item field size for the word, and based on the determination of the data item field size to logically combine the plurality of arithmetic flags of the sets within the word into a single combined arithmetic flag variable of M bits, wherein, in combining, the combination function module performs an OR operation; and

wherein the plurality of arithmetic flags represent a result status of the plurality of data items after a mathematical operation is performed by a processor on the plurality of data items.

2. (Previously Presented) The device recited in claim 1, further comprising:

a condition check module that determines the result status of the combined arithmetic flag variable and causes the processor to execute an appropriate operation based on the result status.

3. (Previously Presented) The device recited in claim 1, wherein the field size is based on either a nibble, byte, half word, or word in length.

4. (Original) The device recited in claim 3, wherein the plurality of arithmetic flags further comprise:

a negative data value, a zero data value, a carry out occurrence in a data value, or an overflow condition in a data item in the plurality of data items.

5. (Canceled)

6. (Previously Presented) The device recited in claim 2, wherein the result status determined by the condition check module further comprises:

any data item has overflowed;

any data item has not overflowed;

any data item is positive or zero;

any data item is negative;

any data item is zero;

any data item is not zero;

any data item has a carry out;

any data item does not have a carry out;

all data items have overflowed;

all data items have not overflowed;

all data items are positive or zero;

all data items are negative;

all data items are zero;

all data items are not zero;

all data items have a carry out; and

all data items do not have a carry out.

7. (Currently Amended) A method of combining a plurality of arithmetic flags for presentation to a processor, comprising:

determining a field size of the plurality of arithmetic flags on which to base a combination process, wherein the plurality of arithmetic flags represent a result status of a plurality of data items after a mathematical operation is performed by the processor on the plurality of data items;

extracting the plurality of arithmetic flags based on the field size;

logically combining the plurality of arithmetic flags based on a function selected when a combination process is selected, wherein the function comprises an OR operation; and

storing a result of the combining of the plurality of arithmetic flags in a destination register for access by the processor.

8. (Previously Presented) The method recited in claim 7, wherein the field size is based on either a nibble, byte, half word, or word in length.

9. (Original) The method recited in claim 8, wherein the plurality of arithmetic flags further comprise:

a negative data value, a zero data value, a carry out occurrence in a data value, or an overflow condition in a data item in the plurality of data items.

10. (Canceled)

11. (Currently Amended) The method recited in claim 7 [[10]], wherein the function may be used to determine the result status of the plurality of data items, said result status comprising:

any data item has overflowed;

any data item has not overflowed;

any data item is positive or zero;

any data item is negative;

any data item is zero;

any data item is not zero;

any data item has a carry out;

any data item does not have a carry out;

all data items have overflowed;

all data items have not overflowed;

all data items are positive or zero;

all data items are negative;

all data items are zero;

all data items are not zero;

all data items have a carry out; and

all data items do not have a carry out.

12. (Currently Amended) An apparatus comprising a data storage medium for storing instructions, wherein the instructions, when executed by a processor, result in the processor performing a method, the method comprising:

determining a field size of the plurality of arithmetic flags on which to base a combination process, wherein the plurality of arithmetic flags represent a result status of a plurality of data items after a mathematical operation is performed by the processor on the plurality of data items;

extracting the plurality of arithmetic flags based on the field size;

logically combining the plurality of arithmetic flags based on a function selected when a combination process is selected, wherein the function comprises an OR operation; and

storing a result of the combining of the plurality of arithmetic flags in a destination register for access by the processor.

13. (Previously Presented) The apparatus recited in claim 12, wherein the field size is based on either a nibble, byte, half word, or word in length.

14. (Original) The apparatus recited in claim 13, wherein the plurality of arithmetic flags further comprise:

a negative data value, a zero data value, a carry out occurrence in a data value, or an overflow condition in a data item in the plurality of data items.

15. (Canceled)

16. (Currently Amended) The apparatus recited in claim 12 [[15]], wherein the function may be used to determine the result status of the plurality of data items, said result status comprising:

any data item has overflowed;

any data item has not overflowed;

any data item is positive or zero;

any data item is negative;

any data item is zero;

any data item is not zero;

any data item has a carry out;

any data item does not have a carry out;

all data items have overflowed;

all data items have not overflowed;

all data items are positive or zero;

all data items are negative;

all data items are zero;

all data items are not zero;

all data items have a carry out; and

all data items do not have a carry out.

17-22. (Canceled)

23. (Currently Amended) A system to manage a plurality of arithmetic flags, wherein an M-bit set of arithmetic flags is associated with each of a plurality of data items of varying field sizes within words of N bits, ~~an N-bit word,~~ M and N being positive integers, comprising:

a combination function module to examine one of the N-bit words ~~a word~~ comprising a plurality of sets of arithmetic flags, to determine a data item field size for the word, and based on the determination of the data item field size to logically combine the plurality of arithmetic flags of the sets within the word into a single combined arithmetic flag variable of M bits, wherein, in combining, the combination function module performs an OR operation; and wherein the plurality of arithmetic flags represent a result status of the plurality of data items after a mathematical operation is performed by a processor on the plurality of data items; and

a processor including a condition check module coupled to the combination function module, the processor to receive the single combined arithmetic flag variable and to determine the next operation to perform based upon the result status of the single combined arithmetic flag variable.

24. (Previously Presented) The system of claim 23, wherein the processor includes at least three stages of pipelining.

25. (Previously Presented) The system of claim 24, wherein the at least three stages of pipelining include a fetch stage, a decode stage, and an execute stage.